place the claim in independent form essentially incorporating the subject matter of independent claim 1. Accordingly, withdrawal of the Examiner's rejection is respectfully requested.

Further, Applicants have amended claim 3 to place it in independent form, essentially incorporating the subject matter of independent claim 1. As claim 3 has been amended to overcome the rejection under 35 U.S.C. § 112, and as claim 3 has not been rejected over prior art, independent claim 3 is believed to be in condition for allowance. Specifically, none of the prior art of record teach or suggest a transistor where a source-end-drain region of the insulated gate transistor is stacked above a channel portion, as shown in Fig. 8 of the present application for example. Accordingly, withdrawal of the Examiner's rejection and allowance of claim 3 is respectfully requested.

PRIOR ART REJECTIONS

The Examiner has rejected claims 1, 4 and 5 under 35 U.S.C. § 102(e) as being anticipated by Mitani et al. This rejection is respectfully traversed.

ALLOWABLE SUBJECT MATTER

The Examiner has objected to claims 2 and 6, indicating that they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, each of claims 2 and 6 has been amended to essentially incorporate the subject matter of independent claim 1. Accordingly, each of claims 2 and 6, and all claims dependent thereon, are believed to be allowable over the

prior art of record. By canceling claim 1, and by amending claims 2 and 6, the Examiner's rejection of claims 1, 4 and 5 is essentially rendered moot.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 2-6 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Donald J. Daley, Reg. No. 34,313.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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MARKED UP VERSION OF CLAIMS

2. (Amended) [The] An insulated gate transistor [according to Claim 1] having a gate electrode on a substrate with a gate insulator interposed therebetween, wherein the gate insulator including silicon and oxygen contains both nitrogen atoms and halogen atoms, and wherein nitrogen atom concentration of the gate insulator is not less than 1×10^{20} cm^{-3}.

3. (Amended) [The] An insulated gate transistor [according to Claim 1], having a gate electrode on a substrate with a gate insulator interposed therebetween, wherein the gate insulator including silicon and oxygen contains both nitrogen atoms and halogen atoms, and wherein a source-and-drain region of the insulated gate transistor is stacked [to upper than] above a channel portion.

4. (Amended) The insulated gate transistor according to Claim [1]2, wherein the insulated gate transistor comprises a floating gate electrode and a control gate electrode provided on the floating gate electrode with an interlayer insulator interposed therebetween.

5. (Amended) The insulated gate transistor according to Claim [1]4, wherein the halogen atom is fluorine.

6. (Amended) [The] An insulated gate transistor [according to Claim 1], having a gate electrode on a substrate with a gate insulator interposed therebetween, wherein the gate insulator including silicon and oxygen contains both nitrogen atoms and halogen atoms, and wherein film thickness of the gate insulator is not less than 0.5 nm and not more than 5 nm.